REMARKS

This communication responds to the Final Office Action mailed on July 24, 2009. Claims 1, 5, 8, 12, 17, 22, 31, and 38 are amended, no claims are canceled, and no claims are added. As a result, claims 1-44 remain pending in this application. The amendments are fully supported in the application as originally filed, for example, at FIGS. 3 & 6, p. 16, line 14 through p. 17, line 22 and p. 19, line 14 through p. 20, line 2. Thus, no new matter has been added.

Moreover, Applicant believes that the amendments would not necessitate any new searching on the part of the Examiner and that the amendments are being made for purposes of placing the present application in condition for allowance. Therefore, Applicant respectfully requests that the amendments be entered for the record.

§103 Rejection of the Claims

Claims 1-44 were rejected under 35 U.S.C. § 103(a) as being unpatentable in view of Hughes et al. (U.S. 6,427,193, hereinafter "Hughes"), Sachs et al. (U.S. 2002/0009067, hereinafter "Sachs") and Ghose et al. (U.S. 2002/0004842, hereinafter "Ghose"). Since a *prima facie* case of obviousness with respect to independent claims 27 and 34 and to amended independent claims 1, 5, 8, 12, 17, 22, 31, and 38 has not been properly established, this rejection is respectfully traversed.

Claims 1, 5, 8, 12, 17, 22, 31, and 38 have been amended to make it clear that the negative acknowledgement comes from the memory resource. Claims 27 and 34 already make it clear that the negative acknowledgement comes from a place other than the processor requesting access to the memory resource.

A conventional system having multiple processors attempts to access a same memory line in a shared memory resource. Typically, the access request by one processor is granted, while the access requests by the other processors are denied. In the conventional system, the processors whose accesses to the same memory line were denied continue to request access to such data until the access is granted. Accordingly, as noted in the Background of the present patent application at p. 3, lines 13-15, "system resources become congested with the multiple

retry requests for access to [the] data, which includes multiple access requests and NACKS in response to such requests." To solve such a problem, the apparatus, system, method and computer-readable medium in the claimed subject matter detect congestion as multiple retry requests attempt to access a shared memory resource. Congestion is detected based on the types of responses (NACKs or ACKs) to the access requests. When congestion is detected, retry logic associated with the multiprocessors stops the processors from attempting access again for a given time period, giving the system time to handle the previous memory request and alleviating memory access congestion.

In contrast, the load/store unit in Hughes is configured to back off from retrying access whenever its associated processor loses sufficient ownership of a particular cache line. Hughes does not detect congestion in memory requests to the same cache line, much less detecting congestion based upon NACKS as described by Applicant and claimed in claims 1-44. Sachs and Ghose discuss, at most, congestion in a network, and not congestion in a memory resource, much less detecting congestion between memory requests to the same memory resource. Finally, none of the cited documents detects congestion in the manner taught and claimed by Applicant in claims 1-44.

Independent claims 1, 5, and 8:

Amended independent claim 1 recites, in pertinent part:

> *a load/store unit that includes a retry logic that is to retry access to a memory resource operatively coupled to the apparatus after receipt from the memory resource of a negative acknowledgment for an attempt to access the memory resource by the load/store unit; and*
>
> *a congestion detection logic to output a signal that indicates that the memory resource is congested based on receipt from the memory resource of a consecutive number of negative acknowledgments in response to access requests to the memory resource.*

Applicant respectfully submits that neither Hughes nor Sachs nor Ghose, alone or in combination, teaches or suggests the elements as recited in amended independent claim 1.

Hughes discusses a "load/store unit ... configured to signal bus interface unit to back off ... [from] attempting to reestablish ownership of a cache line for which ownership was lost via a snoop operation." Hughes, col. 39, lines 20-35. Hughes does not, however, teach that the load/store unit operates to retry access in response to receipt of a negative acknowledgement. Therefore, Hughes fails to show "a load/store unit that includes a retry logic that is to retry access to a memory resource ... after receipt from the memory resource of a negative acknowledgment for an attempt to access the memory resource by the load/store unit," as recited in amended independent claim 1. In addition, as admitted in the Final Office Action at p. 3, lines 4-8, Hughes fails to show "a congestion detection logic to output a signal that indicates that the memory resource is congested based on receipt from the memory resource of a consecutive number of negative acknowledgments in response to access requests to the memory resource," as recited in amended independent claim 1.

Sachs discusses adapting to congestion in a network between a user equipment and a radio base station. *See* Sachs, paragraphs [0028], [0038] and [0044]. Accordingly, Sachs fails to show "a load/store unit ... to retry access to a memory resource," much less "a load/store unit ... to retry access to a memory resource after receipt from the memory resource of a negative acknowledgment for an attempt to access the memory resource by the load/store unit," as recited in amended independent claim 1.

In addition, Sachs teaches that "if a negative acknowledgment as an indication of congestion is returned from the network, the user equipment uses a longer "Subsequent Backoff Delay 2" to ease the load on the [network] channel." Sachs, paragraph [0052], lines 13-18. That is, under Sachs' approach, the user equipment does not detect the congestion based on the negative acknowledgement. In fact, the user equipment in Sachs merely detects collision in a network (a physical process) and reacts to back off from further transmission onto the network for a predetermined period of time. This is the well-known collision detection mechanism used in networks such as the Ethernet network. There is no detection of negative acknowledgements as required by claims 1-44. The negative acknowledgement noted in paragraph [0052] in Sachs is simply the detection by the source node that it is unable to drive its packet onto the network either due to collision or the presence of other traffic. There is no "receipt from the memory resource of negative acknowledgements," as required by claims 1-44. Furthermore, Sachs does

not describe that the congestion in the network is caused by multiple retry requests to access a memory resource. Therefore, Sachs fails to show "a congestion detection logic to output a signal that indicates that the memory resource is congested based on receipt from the memory resource of a consecutive number of negative acknowledgments in response to access requests to the memory resource," as recited in amended independent claim 1.

Ghose discusses coping with congestion in a network. *See* Ghose, paragraph [0117], lines 15-16. In particular, Ghose discusses "network congestion as evidenced by ... the generation of a predetermined number of NACKs ... during a predetermined time interval." Ghose, paragraph [0117], last six lines. However, Ghose does not teach a load/store unit to retry to access to a memory resource after receipt from a memory resource of a negative acknowledgement, or a logic to detect congestion in a memory resource based on receipt from the memory resource of negative acknowledgements. Therefore, Ghose fails to show "a load/store unit ... to retry access to a memory resource ... after receipt from the memory resource of a negative acknowledgment for an attempt to access the memory resource by the load/store unit" and "a congestion detection logic to output a signal that indicates that the memory resource is congested based on receipt from the memory resource of a consecutive number of negative acknowledgments in response to access requests to the memory resource," as recited in amended independent claim 1.

The arguments in favor of patentability of claim 1 similarly apply to amended independent claims 5 and 8, which recite similar limitations.

Independent claims 12, 17, 22, 31, and 38:

Amended independent claim 12 recites, in pertinent part:

> *a congestion detection logic to detect congestion of access to the data from the cache memory based on receipt from the cache memory of a consecutive number of negative acknowledgments in response to the access requests.*

For the same reasons as have been noted with respect to amended independent claims 1, 5, and 8, Applicant respectfully submits that neither Hughes nor Sachs nor Ghose, alone or in combination, teaches or suggests the elements as recited in amended independent claim 12. The

arguments in favor of patentability of claim 12 similarly apply to amended independent claims 17, 22, 31, and 38, which recite similar limitations.

Independent claims 27 and 34:

Independent claim 27 recites, in pertinent part:

> receiving, by the first processor, a positive acknowledgment or a negative acknowledgment from a second processor that is associated with the memory based on one of the number of access requests; and
>
> detecting congestion of the data in the memory based on receipt, by the first processor, of a consecutive number of negative acknowledgments that exceed a first threshold, prior to receipt, by the first processor, of a positive acknowledgment.

Applicant respectfully submits that neither Hughes nor Sachs nor Ghose, alone or in combination, teaches or suggests the elements as recited in independent claim 27. In particular, combination of the cited documents does not show "receiving, by the first processor, a positive acknowledgment or a negative acknowledgment from a second processor that is associated with the memory" or "detecting congestion of the data in the memory based on receipt, by the first processor, of a consecutive number of negative acknowledgments [received from the second processor] that exceed a first threshold, prior to receipt, by the first processor, of a positive acknowledgment," as recited in independent claim 27. The arguments in favor of patentability of claim 27 similarly apply to independent claim 34, which recites similar limitations.

For at least the reasons stated above, Applicant respectfully submits that the Office Action fails to show a prima facie case of obviousness with respect to independent claims 1, 5, 8, 12, 17, 22, 27, 31, 34 and 38, and that these claims are in condition for allowance. Therefore, reconsideration and allowance of independent claims 1, 5, 8, 12, 17, 22, 27, 31, 34 and 38 are respectfully requested. Claims 2-4, 6, 7, 9-11, 13-16, 18-21, 23-26, 28-30, 32, 33, 35-37, 39 and 40 are allowable as depending from their respective independent claims 1, 5, 8, 12, 17, 22, 27, 31, 34 and 38, which are submitted to be allowable.

CONCLUSION

It is respectfully submitted that the claims are in condition for allowance, and notification to that effect is earnestly requested. The Examiner is invited to telephone the undersigned at (612) 373-6909 to facilitate prosecution of this application.

If necessary, please charge any additional fees or credit overpayment to Deposit Account No. 19-0743.

Respectfully submitted,

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CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence is being filed using the USPTO's electronic filing system EFS-Web, and is addressed to: Mail Stop AF, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on November 24, 2009.

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